REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Final Office Action of August 4, 2005 (hereinafter "Final Action"). In response to the additional analysis provided in the Final Action, Applicants provide herein new arguments showing that the cited references fail to disclose or suggest, at least, all of the recitations of the pending independent claims; therefore, Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 1 and 11 are Patentable

Independent Claims 1 and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 5,450,365 to Adachi (hereinafter "Adachi") in view of Japanese Patent No. JP404271673 to Kaneko (hereinafter "Kaneko"). Independent Claim 1 is directed to a memory interface system and recites:

> at least one channel line that couples a memory to a memory controller, the at least one channel line being responsive to a terminal voltage that is independent of a memory supply voltage and a memory controller supply voltage.

Independent Claim 11 includes similar recitations. As illustrated in FIG. 1, for example, of the present Specification, a memory interface system is shown in which the terminal voltage VTER is independent of the memory supply voltage VDD1 and the memory controller supply voltage VDD2. The Final Action alleges that Adachi discloses a memory controller 10 that is responsive to an independent 5V supply voltage, and channel lines 122 and 124 that are responsive to the 3V supply voltage when the switch 26 is configured appropriately, which is independent of the 5V supply voltage and the memory card 14 supply voltage. Kaneko is cited for the proposition that the memory card 14 can be independently powered. (Final Action, page 2).

Applicants respectfully disagree with this interpretation of the teachings of Adachi. In particular, Applicants submit that the voltage powering the channel lines 122 and 124 is not independent of the supply voltage for the memory card 14. In fact, Applicants submit that the voltage powering the channel lines 122 and 124 is dependent on the supply voltage

that powers the memory card 14 in that these voltages will always be the same. Adachi explains this dependence as follows:

> The memory card control device 16 having the above construction will be operated as follows. To begin with, assume that a memory card 14 whose rated supply voltage is 5 volts is mounted on the camera 1 via the connector 12. **On detecting a supply voltage matching the memory card 14, the switch 26 is brought into a condition opposite the condition shown in the FIGURE; that is, the 5-volt connection line 130 is connected to the connection line 120 via the switch 26.** As a result, the supply voltage of 5 volts is applied to the input 120 of the level shifter 20 via the switch 26. (Adachi, col. 4, line 65 – col. 5, line 7).

Thus, according to Adachi, even if the memory card 14 supply voltage is independent of the voltage used to power the channel lines 122 and 124, the voltage used to power the channel lines 122 and 124 is not independent of the memory card 14 supply voltage. Instead, the memory card control device 16 detects the supply voltage for the memory card 14 and uses that same voltage to power the channel lines 122 and 124.

Accordingly, for at least the foregoing reasons, Applicants respectfully submits that independent Claims 1 and 11 are patentable over Adachi in view of Kaneko and that Claims 2 – 10 and 12 - 20 are patentable at least per the patentability of independent Claims 1 and 11.

Independent Claims 1 and 11 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 6,078,978 to Suh (hereinafter "Suh") in view of U. S. Patent No. 6,185,145 to Merritt (hereinafter "Merritt") and U. S. Patent No. 6,184,737 to Taguchi (hereinafter "Taguchi"). The Office Action alleges that when the teachings of the Suh, Merritt, and Taguchi references are combined, independent Claims 1 and 11 are rendered obvious. (Final Action, pages 13 and 14).

Applicants respectfully disagree with this interpretation of the teachings of Suh, Merritt and Taguchi. Turning first to Suh, Applicants acknowledge that Suh describes a bus interface circuit shown in FIG. 1 in which a reference voltage Vref is generated based on a terminal voltage Vtt using an off-chip network of resistors R1 and R2 (Suh, col. 2, lines 1 – 20). Applicants submit, however, that Suh appears to be silent with regard to the voltage source used to power the memory device that the bus interface circuit is used with.

Turning next to Taguchi, this reference discloses a bus transmission system in FIGS. 7 and 9 in which the transmission lines 10 and 11 are responsive to the voltage Vtt. Taguchi,

however, appears to be silent with respect to what voltage is used to power the devices that are to be coupled to the input and output buffers 33 and 32. That is, if these devices are a memory controller and a memory, Taguchi does not provide any teaching with respect to whether voltage Vtt used to power the transmission lines 10 and 11 is independent of the voltages used to power a memory controller and a memory, for example.

Turning next to Merritt, Applicants acknowledge that this reference discloses a memory controller (logic section 200) and a memory 20. However, even if the bus circuits of Suh and Taguchi were to be incorporated into the system of system of Merritt, the combination would not provide a system in which the terminal voltage used to power a channel line is independent of a memory supply voltage and a memory controller supply voltage. As shown in FIG. 1 of Merritt, the voltage VCC2 used to power the logic section 200 must be provided to the buffer 10 so that VREF may be generated based on the voltage VCC2 and a comparison can be made whether the data signal VIN is a logic 0 or a logic 1. (Merritt, col. 4, lines 21 – 44). If an independent voltage is used to power the buffer 10, then the signal comparator 15 would be incapable of making a determination of whether the data signal VIN is a logic 0 or a logic 1.

In view of the analysis above, Applicants respectfully submit that Suh, Merritt, and Taguchi, either alone or in combination, do not disclose or suggest a channel line that is responsive to a terminal voltage that is independent of a memory supply voltage and a memory controller supply voltage as recited in Claims 1 and 11.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 1 and 11 are patentable over Suh in view of Merritt and Taguchi and that Claims 2 – 10 and 12 - 20 are patentable at least per the patentability of independent Claims 1 and 11.

Dependent Claims 10 and 20 are Separately Patentable

Applicants respectfully submit that dependent Claims 10 and 20 are patentable over the cited references for at least the reasons set forth above with respect to Claims 1 and 11. Dependent Claims 10 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Suh in view of Merritt and Taguchi. Dependent Claims 10 and 20 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over Adachi in view of Kaneko and Taguchi.

Claims 10 and 20 recite that the magnitude of the terminal voltage is greater than the magnitudes of the memory supply voltage and the controller supply voltage, respectively. Applicants submit that none of the cited references disclose or suggest using a terminal voltage that has a magnitude greater than the magnitudes of the memory supply voltage and the controller supply voltage, respectively, as recited in Claims 10 and 20.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that dependent Claims 10 and 20 are separately patentable over Suh, Merritt, Kaneko, and Taguchi.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,

D. Scott Moore
Registration No. 42,011

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 6, 2006

Name: Carol L. Rizzo